P87LPC76x Low Pincount Microcontrollers

Programming Specifications

1999 Feb 18

Philips Semiconductors

PHILIPS

1. PINOUT

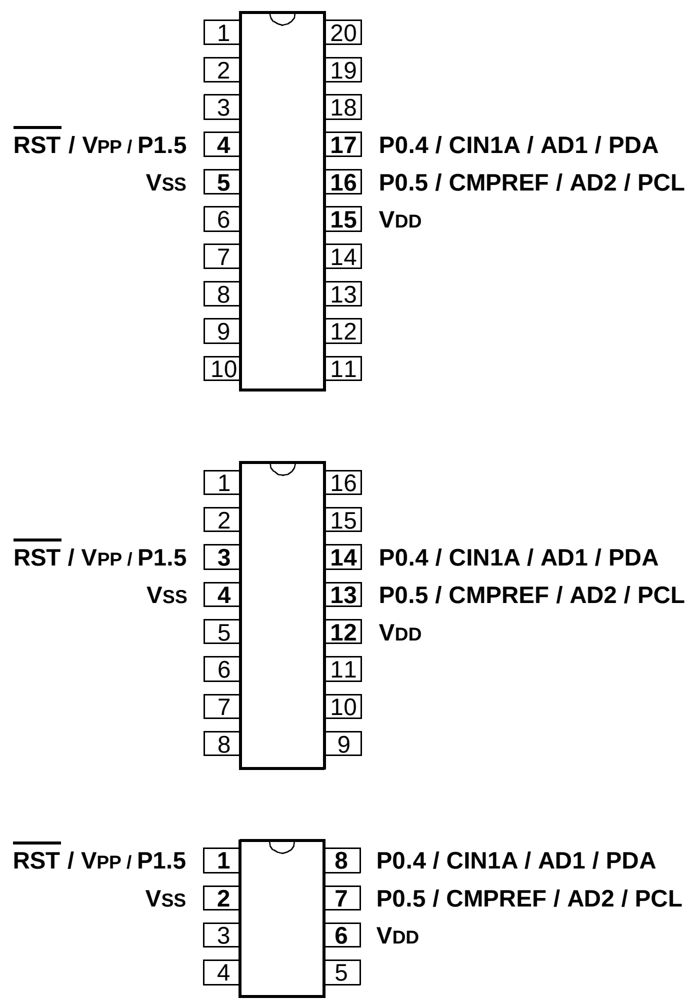


Figure 1: 20, 16, 8 pins DIP pinout

The 20 pin SO package outlines **SOT163-1** is attached at the end of this document.

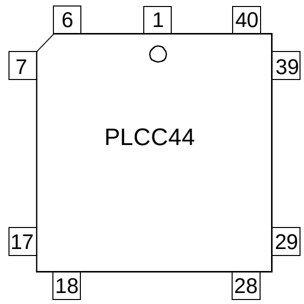


Figure 2: 44 pins PLCC bondout chip

PIN	FUNCTION	PIN	FUNCTION
1	**VSS**	44	
2		43	
3		42	
4		41	
5		40	
6		39	
7		**38**	**P0.4/CIN1A/AD1/PDA**
8	**P1.5/$\overline{\text{RST}}$/VPP**	**37**	**P0.5/CMPREF/AD2/PCL**
9		36	
10	**VSS**	35	
11		34	
12		33	
13		32	
14		**31**	**VDD**
15		30	
16		29	
17		28	
18		27	
19		26	
20		25	
21		24	
22		**23**	**VDD**

Table 1: 44 PLCC pinout (programming related pins are in bold text)

2. PIN DESCRIPTIONS

MNEMONIC	44 pins package PIN NO.	20 pins package PIN NO.	16 pins package PIN NO.	8 pins package PIN NO.	TYPE	NAME AND FUNCTION
VSS	10, 1	5	4	2	P	Ground: 0V reference.
VDD	23, 31	15	12	6	P	Power Supply: 5V +/-.5V
PCL	37	16	13	7	I	Serial clock input for EPROM programming communication.
PDA	38	17	14	8	I/O	Serial data I/O for EPROM programming communication.
VPP	8	4	3	1	P	V_{PP} = 10.75V +/- 0.25V I_{PP} = 30mA during programming.

Table 2: Programming pins in different packages

3. GETTING INTO THE SERIAL PROGRAMMING MODE

1. Disconnect pins PCL and PDA.
2. Connect VDD; the part does not support “hot insertion” into the programming socket
3. Wait 20 uSec (Min) and raise V_{PP} to 10.75V +/- 0.25V; V_{PP} rise time is 1uSec to 100 uSec.

<u>At this point the part is in the programming mode.</u>

4. Wait t_{INIT} = 60 uSec (Min) before beginning the serial communication to the part.
5. Get out of the programming mode by connecting V_{PP} = 0V; V_{PP} fall time is 1uSec to 100 uSec.
6. Disconnect VDD before removing the part from the socket.

The programming mode enables the internal RC oscillator.

During the programming mode PDA and PCL pins are Schmitt trigger inputs.

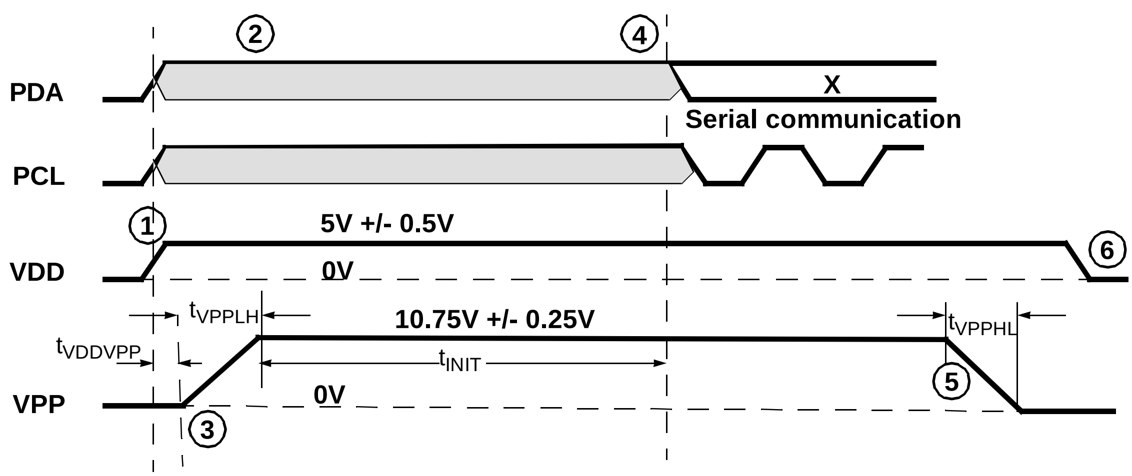


Figure 3: Getting into the programming mode

VDD = 4.5V to 5.5V; V_{PP} = 10.75V +/- 0.25V I_{PP} = 30mA during programming; T_{amb} = 10°C to +40°C

SYMBOL	FIGURE	PARAMETER	LIMITS		UNIT
			MIN	MAX	
t_{VDDVPP}		V_{DD} HIGH to V_{PP} rising edge	20		us
t_{VPPLH}		V_{PP} rise time	1	100	us
t_{VPPHL}		V_{PP} fall time	1	100	us
t_{INIT}		V_{PP} = 10.75V to the beginning of serial communication	60		us

Table 3: Programming mode timings

4. PROGRAMMING MODE

The programming commands are sent by the programmer through the PCL and PDA lines.

Each programming command is one byte shifted into the part by 8 clocks.

The serial interface is identical to the 51's 8-bit serial UART mode 0; LSB is the first bit in the serial byte.

PCL pin is the clock input from the programmer.

PDA pin is the data I/O. Data is enabled on the falling edge of PCL, and is clocked on the rising edge of PCL.

Data output from the part is disabled after the rising edge of PCL for the last bit in a data byte.

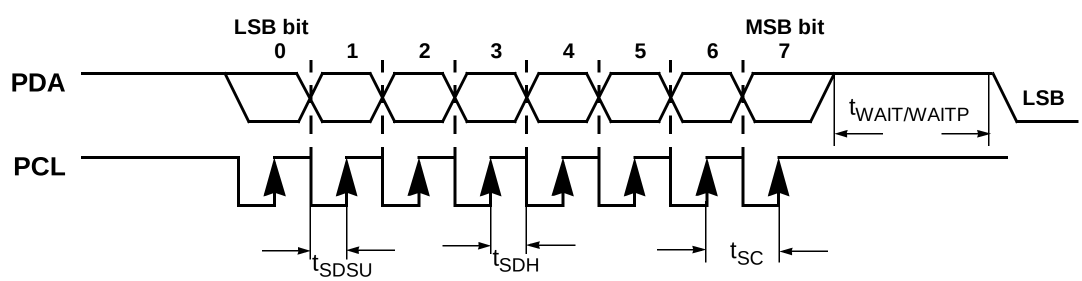


Figure 4: Writing programming commands by the programmer

NAME	OPCODE	FUNCTION
NOP	00H	Not used
LOAD_DATA	02H	Load address counter with the next data byte
RD_DATA	04H	Read data byte addressed by the program counter
INC_ADDR	06H	Increment address counter
LD_ADRR_LO	08H	Load 8 LOW address bits into programming counter
LD_ADRR_HI	0AH	Load 8 HIGH address bits into programming counter
STRT_PRGM	0CH	Start programming a data byte; always followed by the Stopt programming command
STP_PRGM	0EH	Stop programming a data byte; always follows the Start programming command.

Table 4: Programming commands

Notes:

Wait 2 uSec between any two programming commands (except "Start Programming" to "Stop Programming")

Wait 250uSec between "Start Programming" and "Stop Programming" commands.

Example of a sequence of programming commands

LD_ADDR_LO	Wait 2uSec
XX DATA	Wait 2uSec
LD_ADDR_HI	Wait 2uSec
XX DATA	Wait 2uSec
LOAD_DATA	Wait 2uSec
XX DATA	Wait 2uSec
READ_DATA	Wait 2uSec
XX DATA	Wait 2uSec
INC_ADDR	Wait 2uSec
LOAD_DATA	Wait 2uSec
XX DATA	Wait 2uSec
STRT_PRGM	Wait 250uSec
STP_PRGM	Wait 2uSec

Table 5: Sequence of programming commands

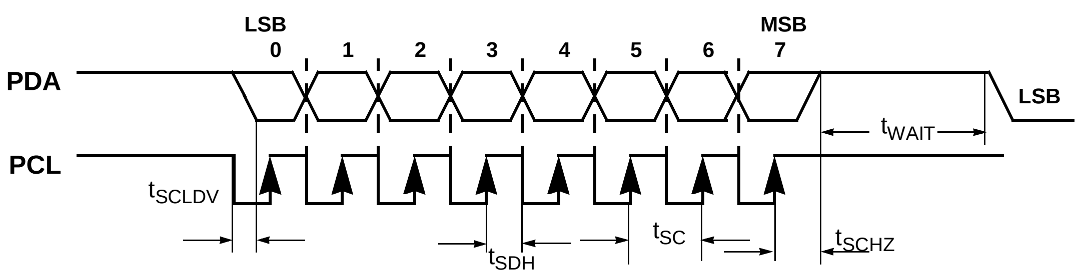


Figure 5: Reading data by the programmer

SYMBOL	FIGURE	PARAMETER	LIMITS		UNIT
			MIN	MAX	
t_{SC}	5	Serial clock cycle time	0.2	1000	us
t_{WAIT}	5	Wait between two serial bytes	2		us
t_{WAITP}	5	Wait after a "Start Programming" command	250		us
t_{SDSU}	4	Serial data setup time to the rising edge of the serial clock	40		ns
t_{SDH}	5	Serial data hold time after the rising edge of the serial clock	10		ns
t_{SCLDV}	5	Serial clock LOW to valid data of the first data bit in a byte		40	ns
t_{SCHZ}	5	Serial clock HIGH to data Hi-Z at the last data bit in a byte		40	ns

Table 6: Programming commands timing

Address	Memory Definition
0000H to 0FFFH	User's code; program/read by the programmer
FC30H	Company signature 15H - Read only by programmer
FC31H	Part's signature DDH - Read only by the programmer
FC60H	Derivative's signature 00H - Read only by the programmer
FCE0H to FCFFH	32 bytes used as user's parameters; program/read by the programmer
FD00H	User Configuration Reg. #1 (UCFG1) program/read by the programmer
FD01H	User Configuration Reg. #2 (UCFG2) program/read by the programmer

Table 7: EPROM Mapping

The programmer programs the user's code at address 0 to FFFH and configuration registers located at address FCE0H to FD01H. These configuration registers configure the chip's modes of operation.

5. USER CONFIGURATION REG. #1 (UCFG1) AT ADDRESS FD00H

	7	6	5	4	3	2	1	0
Programmed bits	**WDTE**	**RPD**	**PRHI**	**BO2.5**	**CLKR**	**FOSC2**	**FOSC1**	**FOSC0**
Erased State	**FFH**							

Table 8: User Configuration Register #1

WDTE: WatchDog Timer Enable;

1 = (Erased) WDT enabled

0 = (Programmed) WDT disabled

RPD: Reset Pin Disable;

1(Erased) External Reset pin disabled (The internal power-on reset is enabled)

0 (Programmed) External Reset pin enabled

PRHI: Port Reset High;

1 = Enable ports to high during and after RESET

0 = Enable ports to low during and after RESET

BO2.5: Brown out at 2.5V;

1 = Enable brown out at 2.5V

0 = Enable brown out at 3.8V

CLKR: CLock Rate select;

1 = Enable divide by 1 of clock (6 clocks per machine cycle)

0 = Enable divide by 2 of clock (12 clocks per machine cycle)

FOSC2 - FOSC0: Oscillator control bits;

	FOSC2	FOSC1	FOSC0
External clock input at pin X1	1	1	1
Internal RC clock; 6MHz +/- 25%	0	1	1
32KHz to 100KHz external Crystal/Resonator	0	1	0
100KHz to 4 MHz external Crystal/Resonator	0	0	1
4 MHz to 20 MHz external Crystal/Resonator	0	0	0

Table 9: FOSC2-FOSC0 bit function

6. USER CONFIGURATION REG. #2 (UCFG2 AT ADDRESS FD01H)

	7	6	5	4	3	2	1	0
Programmed bits	**SEC2**	**SEC1**						
Erased State	**FFH**							

Table 10: User Configuration Register #2

SEC2-SEC1: SECurity bits 2 & 1;

11 = Security bits unprogrammed; Programming and Verify allowed.

10 = Security bit 2 unprogrammed; 1 programmed; Programming disabled, Verify enabled.

00 = Both bits programmed; Programming and Verify disabled

7. 32 REGISTERS OF USER’S PARAMETERS (FCE0H TO FCFFH)

The 32 registers of user’s parameters are programmed as code located at address FCE0H to FCFFH.

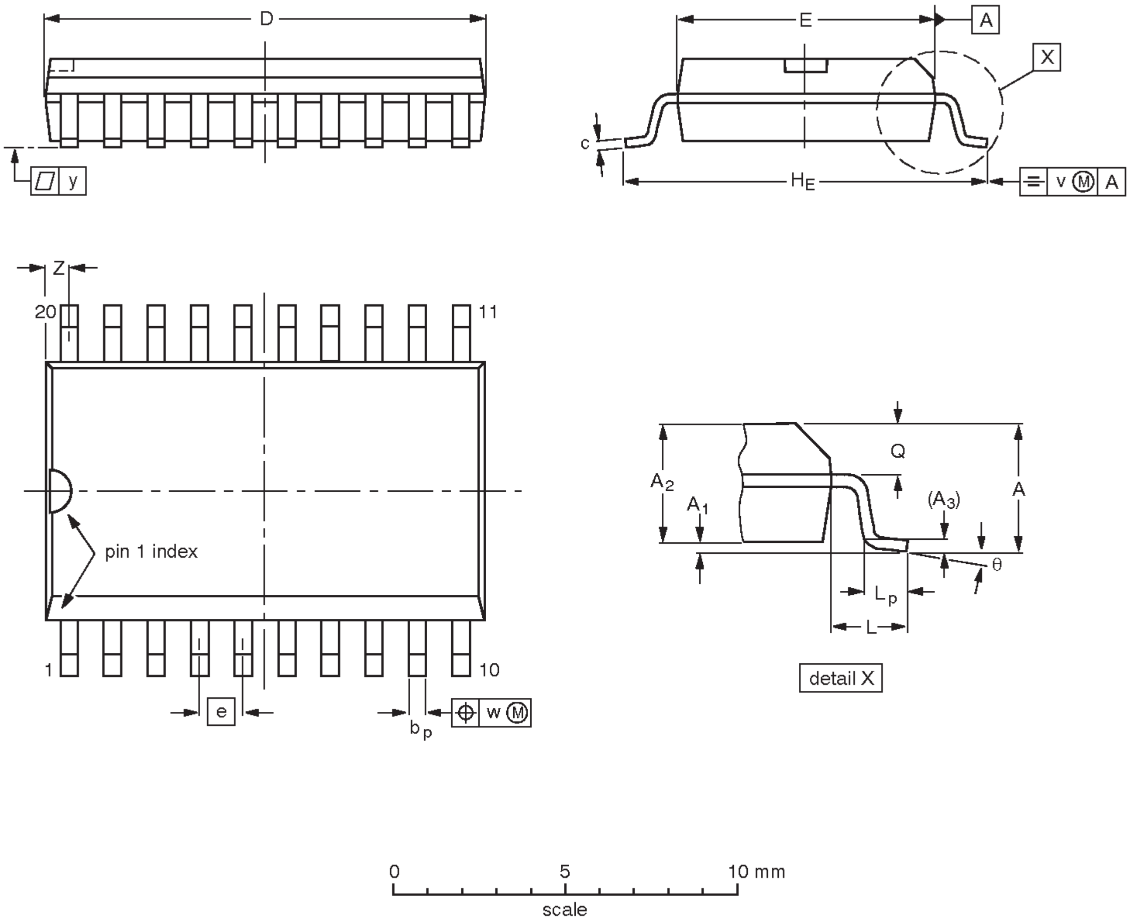
The content of the 32 parameter registers and the two configuration registers are defined by the HEX file at addresses:

FCE0H to FCFFH	32 bytes used as user’s parameters; program/read by the programmer
FD00H	User Configuration Reg. #1 (UCFG1) program/read by the programmer
FD01H	User Configuration Reg. #2 (UCFG2) program/read by the programmer

The user should be able to display, edit, program and verify the two configuration registers and the user’s 32 bytes located at address FCE0H to FCFFH.

Package outlines

SO20: plastic small outline package; 20 leads; body width 7.5 mm SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22